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Structural and Electrical Analysis of Various MOSFET Designs

Pallavi Choudhary*, Tarun Kapoor**
*Department of Electronics & Communication Engineering, SBITM, Betul
**Department of Electronics & Communication Engineering, UIET, CSJMU, Kanpur.

ABSTRACT
Invention of Transistor is the foundation of electronics industry. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the key to the development of nano electronics technology. This paper offers a brief review of some of the most popular MOSFET structure designs. The scaling down of planar bulk MOSFET proposed by the Moore's Law has been saturated due to short channel effects and DIBL. Due to this alternative approaches has been considered to overcome the problems at lower node technology. SOI and FinFET technologies are promising candidates in this area.
Keywords **–**FD MOSFET, FINFET, PD MOSFET, PLANAR MOSFET, SOI.

I. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistors (MOSFET's) has brought a revolution in the semiconductor industry since its invention in 1960's. Even though it is slower than a bipolar junction transistor, a MOSFET is smaller and cheaper and also uses less power, hence allowing greater numbers of transistors to be packed together. A transistor is generally characterized by its gate length (L) & gate width (W). Gate length is the distance; an electron has to travel from highly doped Source to Drain. X-nm refers to the gate length. Approximately each lower node technology is "0.7 times the previous technology" viz. 130 nm, 90 nm, 65 nm , 45 nm and so on. The 22 nanometer (22 nm) is the next CMOS process step following the 32 nm step on the International Technology Roadmap for Semiconductors (ITRS). Transistor length, width, and the oxide thickness, each scale with a factor of 0.7 per node. Transistor channel resistance does not change with scaling, whereas gate capacitance is reduced by a factor of 0.7. Therefore, the RC delay of the transistor scales with a factor of 0.7. The chips become faster by 17% per year, reduced power consumption.

Smaller MOSFETs are obligatory for several reasons. The most important reason of making transistors smaller is to carton more and more devices in a fixed chip area. This results in a chip with similar functionality in a comparatively small area, or chips with more functionality in the same area. Since fabrication expenses for a semiconductor wafer are relatively fixed, the cost per integrated circuits is primarily related to the number of chips which can be produced per wafer. Hence if the size of IC is small more chips can be manufactured per wafer, hence dropping the price per chip. In fact, since past 30 years the number of transistors per chip has been doubled every 2–3 years on introduction of a new technology node. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as compared to a 65 nm chip. This doubling up of transistor density was first detected by Gordon Moore in 1965 and is frequently referred to as Moore's law.

Along with scaling down of transistors, various types of structures have also been proposed for better functionality and compact size.

II. PLANAR BULK MOSFET

The planar bulk-silicon MOSFET has been the workhorse of the semiconductor industry over the last 40 years. However, the scaling of bulk MOSFETs becomes increasingly difficult for gate lengths below ~32nm (sub-45 nm half-pitch technology node) expected by the year 2009. As the gate length is condensed, capacitive coupling of the channel potential to the source and drain increases relative to the gate, leading to significantly degraded short-channel effects (SCE). This manifests itself as a) increased off-state leakage
b) threshold voltage (VTH) roll-off, i.e., smaller VTH at shorter gate lengths
c) reduction of VTH with increasing drain bias due to a modulation of the source-channel potential barrier by the drain voltage, also known as drain-induced barrier lowering (DIBL)
d) Subtheshold swing

Each of these technologies is now approaching vital physical limitations which may, in turn, limit further scaling of device dimensions.

Schematically shown in Figure 2.1, a MOSFET consists of two back-to-back connected *p-n* junctions. The gate voltage applied across metal-oxide semiconductor (MOS) capacitor creates an inversion channel connecting the source and the drain, and controls the carrier density in it. From an operational point of view, the MOSFET has two critical

structural parameters, namely gate length and gate dielectric thickness. MOSFET scaling affects both lateral and vertical device dimensions. While the reduction of the lateral dimensions increases the transistor density in a chip, the reduction of the oxide thickness is needed to ensure good electrostatic integrity.

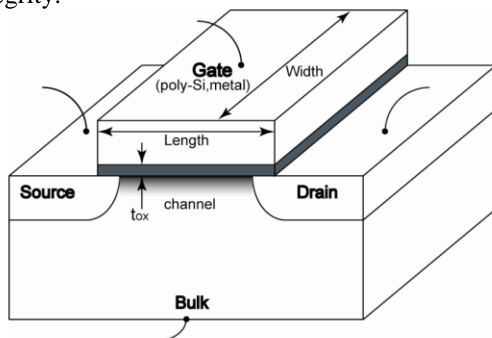


Figure 2.1 Schematic view of a surface-channel

MOSFET device indicating physical gate length, channel width and physical gate dielectric oxide thickness (tox).

In contemporary MOSFETs the drain current *Id* is determined by:

$$\frac{I_d}{W} = C_{ox}(V_G - V_{th})v \quad (1)$$

where *W* is the channel width, *Cox* is the gate capacitance per unit area, and *v* is the source end carrier velocity. The saturation transconductance *gm* may be obtained by

$$\frac{g_m}{W} = \frac{\partial I_d}{\partial V_g}/W = C_{ox} \times v = \frac{\epsilon_{ox}}{t_{ox}} \times v \quad (2)$$

where ε_{ox} is the oxide permittivity. The carrier velocity is usually saturated at short-channel MOSFETs, thus g_m/W is an index of gate oxide thickness t_{ox}. Since gate capacitance per unit area is inversely proportional to oxide thickness, both the device current and the saturation transconductance are closely related to oxide thickness.

In addition, the threshold voltage has also been reduced to maintain appropriate gate voltage overdrive according to equation (1). However, the reduction of supply voltage and threshold voltage has lagged the gate length and gate dielectric thickness scaling. The slower reduction of the threshold voltage is due to a combination of factors including increasing channel doping needed to control short-channel effects. The sub linear threshold voltage scaling in turn has retarded the scaling of the supply voltage.

The MOSFET substrate doping, and especially the channel doping concentration, have been continuously increasing since the beginning of scaling. From the original doping density of approximately 2.5×10^{16} cm^{-3} in 1 μm gate length transistors [2], it has already reached more than 2×10^{18} cm^{-3} in contemporary 35 nm gate length MOSFETs.

In MOS devices, the gate dielectric thickness is the single most important device dimension to enable device scaling and has also been the most aggressively scaled one. A thin gate dielectric increases capacitive coupling from the gate to the channel, thereby reducing the source/drain influence on the channel. A larger gate capacitance also results in a larger inversion charge density, or in other words increased ON-state drive current.

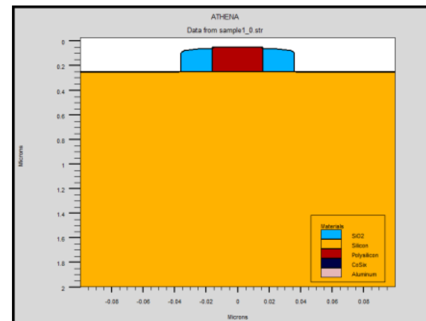


Figure 2.2 Planar Mosfet

The effects due to scaling down are manifested in various ways:

i) Decline of threshold voltage with attenuation of gate length (VT roll-off),

ii) VT reduction with growing drain voltage (drain induced barrier lowering – DIBL),

iii) Degraded subthreshold swing.

Collectively, these phenomena are known as ‘short channel effects’ (SCE) and they tend to increase the off-state static leakage power.

III. SOI MOSFET

Silicon on insulator (SOI) technology uses a layered silicon-insulator-silicon substrate instead of conventional silicon substrates to reduce parasitic device capacitance and thereby improving circuit performance. [3]

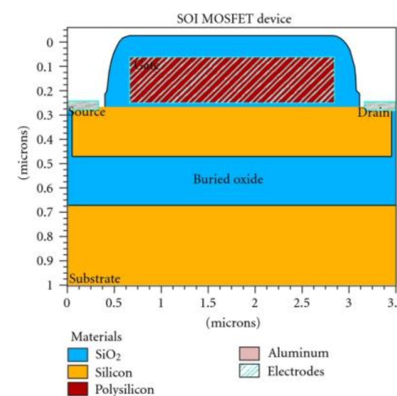
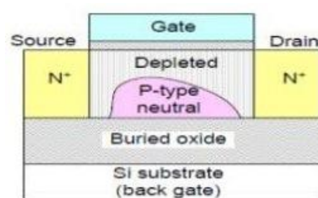


Figure 3.1SOI MOSFET

There are two types of SOI MOSFET viz. partially depleted SOI MOSFET and fully depleted SOI MOSFET.

The fully depleted SOI MOSFETs have a very thin layer of silicon on the top, hence the channel is completely depleted form the majority carriers, hence the name fully depleted. Due to this, the SOI layer is very small as compared to the depletion width of the device. Hence the voltage can be controlled by the gate very effectively.

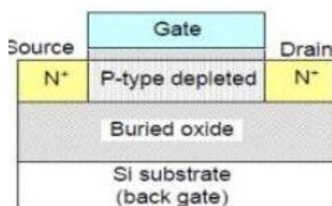
As a result there is no neutral region in the body of the MOSFET that can be charged. The advantage of FD SOI MOSFET is the elimination of the floating-body effect and better short channel behavior.



Partially Depleted SOI

Figure 3.2 Partially Depleted SOI MOSFET

For Partially Depleted SOI MOSFET, the SOI layer thickness is thicker than the maximum depletion width of the gate. Usually the silicon film thickness is more than 50nm, which improves the constraint on device threshold voltage and sensitivity. PD SOI MOSFET structures are easy to manufacture and the process and device design are much more compatible as compared to traditional planar bulk CMOS. In general, PD SOI device is optimal for high speed and is being targeted for applications where highest clock rates are needed. However the major issue of the partially depleted device is the floating body effect.



Fully Depleted SOI

Figure 3.3 Fully Depleted SOI MOSFET

FDSOI MOSFET has lower leakage current than PD SOI MOSFET. The leakage current is inversely proportional to the channel length, gate oxide thickness and threshold voltage. The threshold voltage in PD SOI MOSFET is more than that of FDSOI MOSFET. The main drawback in PDSOI MOSFET is kink effect, which is eliminated in FDSOI MOSFET. [4]

IV. Multi Gate MOSFET

FinFET is the most promising design among all the multi gate MOSFET structures. This structure has a thin silicon body known as fin and gate terminal wrapped around it. FinFET is very easy to fabricate and has multiple gate hence it has been considered as the most important alternative to replace planar MOSFETs by ITRS

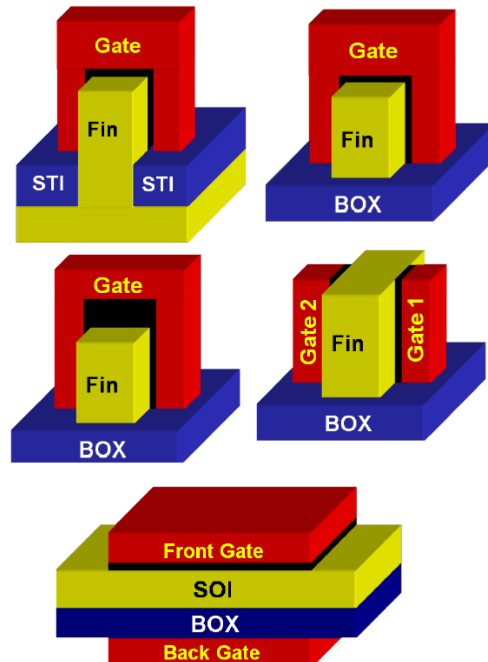


Figure 4.1 Various Structures of Multi Gate MOSFET Devices

This device can be fabricated either over bulk or SOI substrate thereby creating BULK FinFET or SOI FinFET accordingly. If the oxide hard mask on the top of the fin is not removed then double gate FinFET is produced. In this design the top surface of Fin has no current conductivity on the other hand in triple gate FinFETs the top surface as well as the sides conduct current. A FinFET can also be fabricated with two independently biased gates. This can be done by erasing top portion of gate of a conventional FinFET using the technique of chemical mechanical polishing and hence forming independent double gate [5].

V. Conclusions

In this paper, a brief review of all the available MOSFET designs have been presented. By analyzing the structure of all the above designs, it can be concluded that multi gate MOSFETs are advantageous over conventional planar scheme. Moreover SOI technology has brought a revolution in the scaling down of transistors hence packaging more amounts in the same space. FinFET technology is another encouraging opportunity in this industry.

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